

WHAT IS CLAIMED IS:

1. A method for monitoring signal changes on a bus interconnect comprising:

- 5 (a) enabling a signal line debouncing circuit;
- (b) detecting the assertion of a signal change line;
- (c) decoding a debounced signal line; and
- (d) performing an operation associated with a signal on the debounced signal line.

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2. The method of claim 1, wherein the signal change line is a logical combination of a plurality of debouncing circuit outputs and if any one output of the plurality changes, then the signal change line is asserted.

15 3. The method of claim 2, wherein if more than one output of the plurality change, then the debounce line is asserted.

4. The method of claim 1, wherein the detecting step comprising the step of periodically polling the status of the signal change line.

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5. The method of claim 1, wherein when the signal change line is asserted an interrupt is generated, the detecting step comprising the step of receiving the interrupt and initiating processing of the interrupt.

5 6. The method of claim 1 further comprising the step of repeating steps (b)-(d) after completing the performing step.

7. The method of claim 1, wherein the assertion is asserted by the signal line debouncing circuit.

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8. The method of claim 1, wherein there are a plurality of debounced signal lines, and the decoding step comprises the determination of which debounced signal line changed.

15 9. The method of claim 1, wherein the signal line debouncing circuit asserts an interrupt when asserting a signal change line, and the detecting step comprises receiving the interrupt.

10. A signal debouncing circuit comprising:

a memory device coupled to a signal line, the memory device to store
a value based on a signal value on the signal line;

a serially connected sequence of storage devices coupled to the
5 memory device, wherein:

an input of a first storage device is coupled to the memory
device;

an input of subsequent storage devices is selectively coupled
to an output of a previous storage device; and

10 an output of a last storage device provides a debounced
version of the signal value provided to the memory device.

11. The signal debouncing circuit of claim 10, wherein the input of
subsequent storage devices are selectively coupled to the output of a
15 storage device immediately before it in the sequence of storage devices.

12. The signal debouncing circuit of claim 10, wherein the inputs of the
subsequent storage devices are also selectively coupled to the output of the
memory device.

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13. The signal debouncing circuit of claim 10, further comprising a final storage device coupled to the output of the last storage device in the sequence of storage devices, the final storage device to store the debounced signal.

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14. The signal debouncing circuit of claim 13, wherein the inputs of the subsequent storage devices are also selectively coupled to an output of the final storage device.

10 15. The signal debouncing circuit of claim 13 further comprising:
a previous signal value storage device coupled to the output of the final storage device, the previous signal value storage device to save the signal value for an additional clock period; and

a signal change unit having a first input coupled to the output of a
15 final storage device and a second input coupled to the output of a the previous signal value storage device, the signal change unit to compare its inputs and asserting a signal change flag when the inputs are different.

16. The signal debouncing circuit of claim 10, wherein the memory
20 device comprising two flip-flops sequentially connected.

17. The signal debouncing circuit of claim 16, wherein the flip-flops are D-type flip-flops.

18. The signal debouncing circuit of claim 10, wherein the sequence of
5 storage devices comprising a sequence of flip-flops.

19. The signal debouncing circuit of claim 18, wherein the flip-flops are D-type flip-flops.

20. The signal debouncing circuit of claim 10, wherein the final storage
10 device is a flip-flop.

21. The signal debouncing circuit of claim 10, wherein the signal line is a communications bus to carry a plurality of states, and the signal debouncing
15 circuit further comprising a decoder having an input coupled to the communications bus and an output coupled to the memory storage device, the decoder containing circuitry to decode a state on the communications bus and produce a true output should the decoded state match a desired state.

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22. A bus monitor comprising:

a communications bus to carry one of a plurality of states;

a decoder having an input coupled to the communications bus, the decoder containing circuitry to decode a current state of the

5 communications bus;

a plurality of memory storage devices, each memory storage device having an input coupled to the decoder, the memory storage device to store a value provided to it by the decoder;

a plurality of debouncing circuits, each debouncing circuit having an
10 input coupled to one of the plurality of memory storage devices, the debouncing circuit containing circuitry to debounce the value stored in the memory storage device; and

a logic engine coupled to outputs from each debouncing circuit, the logic engine containing circuitry to examine the debounced values and
15 perform prespecified actions based on the debounced values.

23. The bus monitor of claim 22, wherein the decoder produces a true value for a state equal to the current state of the communications bus and a false value for all remaining states.

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24. The bus monitor of claim 22, wherein the bus monitor part of a peripheral is coupled to the bus.

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25. A peripheral comprising:

a communications bus to permit transmission and reception of data;

a bus interface coupled to the communications bus, the bus interface containing circuitry to translate data on the communications bus into a form

5 usable by the peripheral;

an engine coupled to the bus interface, the engine comprising:

a bus monitor coupled to the bus interface, the bus monitor containing circuitry to decode data from the communications bus and perform prespecified actions based on the decoded data; and

10 a signal debouncing circuit coupled to signal pins from the peripheral, the signal debouncing circuit containing circuitry to provide a debounced and stable signal from the peripheral to the engine; and

a microcontroller coupled to the engine, the microcontroller containing circuitry to control the operation of the peripheral.

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26. The peripheral of claim 25, wherein the communications bus is a universal serial bus communications bus.

27. The peripheral of claim 26, wherein the communications bus is a

20 universal serial bus version 2.0 communications bus.

28. The peripheral of claim 25, wherein the communications bus is an IEEE 1394 communications bus.

29. The peripheral of claim 25, wherein the communications bus is a
5 small computer system interface (SCSI) communications bus.

30. The peripheral of claim 25, wherein the communications bus is a PC card communications bus.

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